Analog-to-Digital Converter

Md. Ariful Islam

Id: 1822033043

Department of Electrical & Computer Engineering

North South University

Dhaka, Bangladesh

[islam.ariful18@northsouth.edu](mailto:islam.ariful18@northsouth.edu)

IMRAN AL MUNYEEM

Id: 1310513642

Department of Electrical & Computer Engineering

North South University

Dhaka, Bangladesh

[imran.munyeem@northsouth.edu](mailto:imran.munyeem@northsouth.edu)

Md. Ariful Islam

Id: 1512097643

Department of Electrical & Computer Engineering

North South University

Dhaka, Bangladesh

[ariful.islam@northsouth.edu](mailto:ariful.islam@northsouth.edu)

**I.  Introduction**

An ADC changes over a constant time and nonstop adequacy analogue signal to a discrete-time and discrete abundance digital signal. The change includes quantization of the input, so it essentially presents a modest quantity of error or noise. Besides, rather than constantly playing out the transformation, an ADC does the change occasionally, sampling the input, restricting the suitable bandwidth of the input signal.

The presentation of an ADC is essentially described by its bandwidth and signal-to-noise ratio (SNR). The bandwidth of an ADC will be portrayed basically by its sampling rate. The SNR of an ADC will be affected by numerous factors, including the resolution, linearity, and accuracy (how well the quantization levels coordinate the genuine analogue signal), aliasing, and jitter. The SNR of an ADC is often summed up as far as its effective number of bits (ENOB), the number of bits of each measure it returns that are on normal not noise. A perfect ADC has an ENOB equivalent to its resolution. ADCs will be picked to coordinate the bandwidth and required SNR of the signal to be digitized. On the off-chance that an ADC operates at a sampling rate more noteworthy than double the bandwidth of the signal, at that point per the Nyquist–Shannon sampling theorem, perfect reconstruction is conceivable. The nearness of quantization error restrains the SNR of even a perfect ADC. In any case, if the SNR of the ADC surpasses that of the input signal, its belongings might be dismissed bringing about a perfect digital portrayal of the analogue input signal.

**II.  Literature Review**

Analogue-to-digital converters are a class of data converters with one path change from Analog to Digital domain. An execution of ADC‟s is normally done either as serial or parallel converters. Before changing over a signal to the digital domain, an analogue signal is first changed over to discrete form utilizing Sample and Hold circuit. Next, if the sample is at the same time contrasted with different Quantization levels and changed over to the digital domain in a single step, it has named as Parallel Converter. On the off-chance that the framework looks at the sampled output to the different Quantization levels in serial fashion, it has named as Serial Converter. The Example of Parallel Converter is Flash Converter and that of Serial Converter is Single, Dual Slope, and Successive Approximation Register (SAR). Superior Converters are an exceptional class of Analog-to-Digital Converters with improved attributes. For example, a high Sampling rate in the order of MHz‟s and resolution. This category of converters incorporates Self-calibrating Converters, Pipelined Converters, Delta Sigma Converters, etc.

Some commonly used Analog-to-Digital Converters are as follows:

*A.*       *INTEGRATING TYPE ADC*

1. Single Slope: This Analog to Digital Converter comprises an integrator, a comparator, and a counter. In this sort of Analog to Digital Converter, the input signal will be taken care of to the integrator. The time will be taken by the capacitor to charge, which is proportional to the input voltage, will be resolved. The counter means the equal span as taken by the capacitor to charge. The calculation of the counter gives a rough change estimation of the signal. Figure 1 shows the working of a single slope incorporating ADC. Figure 2 shows the output of the integrator.

**Output**

**Counter**

**-**

**+**

**-**

**+**

**V**

**in**

**Clk**

Fig. 1: Single Slope ADC.

**t**

V

int

**V**

**ref**

Fig. 2: Output of integrator in Single Slope ADC.

The greatest favourable position of this data converter is its formlessness. Other than it gives better resolution however errors are conspicuous. The accuracy of this ADC will be dictated by the estimation of R and C in the integrator. A low-noise CMOS Image Sensor (CIS) in light of a 14-bit Two-Step Single-Slope ADC (TS SS ADC) and a section self-calibration strategy will be proposed, notwithstanding, there are plenty of errors in the circuit activity which make it hard to be actualized. One more shortcoming of this sort of ADC is its huge transformation time (2N cycles).

2. Dual Slope: Figure 3 shows the circuit of Dual slope integrating Analog to Digital Converter. Here the integrating activity will be performed for a fixed period. The value of combination changes relatively with input voltage sampled value. The capacitor is then permitted to release and the counter runs for the discharging period hence changing over the analogue signal to a digital word. Figure 4 shows the integrating and disintegrating waveform.

Dual slope integrating ADC is the highest accurate, low power, high-resolution Data converter. It has the least likelihood of error, for example, maximum noise resistance; thus exactness parts are not required. Its solitary impediment is it's low-speed as it is the slowest Data converter with change time of 2\*2N cycles*.*

**-**

**+**

**-**

**+**

**V**

**in**

**V**

**ref**

**Timer**

**Control**

**Counter**

**Digital**

**Output**

Fig. 3: Dual Slope ADC.

**Charging**

**Time**

**Discharging Time**

**t**

**1**

**t**

**2**

**t**

**3**

**V**

**t**

Fig. 4: Waveform of Dual Slope ADC.

*B*. *Flash ADC*

For conversion of data into N-bit digital word, flash type of ADC utilizes M=2 N comparators and compares the fixed input signal to a varying reference signal. The output of these comparators have taken care of to an M: N encoder to get N-bit data at output. Since M number of comparators work simultaneously, hence otherwise called Parallel Analog to Digital Converter. Figure 5 shows the 8-bit flash Analog to Digital Converter. Flash or Parallel Analog to Digital Converter is the simplest type of Data Converter and takes minimum time, i.e., single cycle time to convert the signal to digital form. Since less time implies more speed, it is reasonable for applications requiring large bandwidth. The only limitation of Flash ADC is 2 N comparators have utilized, because of which it becomes expensive and power inefficient.

**8**

**:**

**3**

**Encod**

**er**

**Vin**

**Vref**

**Digital**

**Output**

Fig. 5: Flash/Parallel Converter

According to the momentum explore the situation, work is advancing of performance of quickest single-core ADC. So far the speed of Flash ADC has expanded up to the ultra-high scope of 24 GS/s in 28nm low power digital CMOS, anyway, there is an exchange off with resolution that has diminished to 3 bits. The fast and better resolution has acquired utilizing Hybrids. A high-resolution (14 bits), medium sampling rate (200MS/s) at low power has structured utilizing a pipelined Flash SAR ADC design by utilizing associated level-shifting (CLS), go scaling also, capacitor sharing procedures.

*C. SUCCESSIVE APPROXIMATION REGISTER ADC*

SAR ADC works on an equivalent principle as that of Ramp

ADC. but rather than employing a digital counter beginning at zero, it uses an artificial approximation register that counts by trying all bits ranging from the most significant bit. Here the comparison has finished by setting the most significant bit ‘1’ and every one alternative bit ‘0’ and therefore the worth of the most significant bit has set. within the next cycle, the second the most significant bit is ready ‘1’ and next bits ‘0’ and therefore the second the most significant bit is therefore determined so on. Figure 6 shows the diagram of SAR ADC.

**Digital**

**logic**

**SAR**

**Comp**

**DAC**

**Analog**

**Input**

**Digital Output**

Fig. 6: SAR ADC.

SAR consumes less time to operate as compared to Ramp ADC. SAR is known for being power economical, its power consumption price has faded to ultra-low aim bound areas. The reduction in power consumption has achieved up to nano-watt vary at the price of resolution. By reducing the binary search vary 83% power saving has achieved at 1 Volt offer voltage. to urge a versatile design designer has got to think about the trade-off between resolution, power, and sampling speed. analysis conducted to enhance rate or resolution will increase power consumption to micro-watt vary, e.g., an 11-bit 40KS/s SAR ADC achieves 10.75 effective range of bit (ENOB) and consumes 10μW as per a recently planned model. The shortcomings of SAR embrace high system quality and its value is larger than counter sort ADC.

**III. CONCLUSION**

Various ADCs are given during this paper similar to Flash ADC works with most speed however consumes massive area and has a low resolution. Similarly, SAR can accustom to attain ultra-low-power at the value of either resolution or speed and dual Slope consumes minimum power. Hence there is a trade-off between numerous performance parameters like resolution, sampling speed, power consumption, area, and others relying upon the applying demand. For medicine implants, parenthetically, the system ought to work at moderate speed, low power consumption, thus a SAR or a dual-slope is appropriate to use.

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